WHAT IS CLAIMED IS:

1. A switching element comprising:

a first port comprising a plurality of lines;

a second port comprising a plurality of lines;

a third port comprising a plurality of lines;

a first memory cell including a storage element, a first pass gate for selectively coupling a first line of said first port to said storage element, a second pass gate for selectively coupling a first line of said second port to said storage element, and a third pass gate for selectively coupling a first line of said third port to said storage element; and

a second memory cell including a storage element, a first pass gate for selectively coupling a second line of said first port to said storage element, a second pass gate for selectively coupling a second line of said second port to said storage element, and a third pass gate for selectively coupling a second line of said third port to said storage element.

2. The switching element of Claim 1 wherein the first and second ports comprise output ports for reading data from said storage elements of said memory cells and said third port comprises an input port for writing data to said storage elements of said memory cells.

3. The switching element of Claim 1 wherein the first and second ports comprise input ports for reading data from said storage elements of said memory cells and said third port comprises an output port for writing data to said storage elements of said memory cells.

4. The switching element of Claim 1 wherein said storage elements comprise capacitors.

5. The switching element of Claim 1 wherein said pass gates comprise field effect transistors.

6. A switch comprising:

a plurality of port blocks each comprising:

a plurality of I/O ports; and

a plurality of memory cells each including a first pass gate for coupling a selected line of the first port with a storage element and a second pass gate for coupling a selected line of the second port with said storage element;

read decoder circuitry for selecting one of said plurality of I/O ports of a first selected one of said plurality of port blocks and reading data from a selected memory cell of said second selected port block; and

write decoder circuitry for selecting one of said plurality of I/O ports of a second selected one of said plurality of port blocks and writing data into a selected memory cell of said second selected port block.

7. The switch of Claim 6 wherein said read decoder comprises a demultiplexer selectively coupling an output port to said selected one of said plurality of I/O ports of said first selected port block.

8. The switch of Claim 6 wherein said read decoder comprises a multiplexer selectively coupling an input port with a selected one of said plurality of I/O ports of said second selected port block.

9. The switch of Claim 6 wherein said plurality of port blocks are organized as an array of N number of rows and M number of columns, each of said port blocks having K number of P-bit wide output ports and said read decoder comprises:

for each of said N number of rows, M number of K x 1 multiplexers each for selecting one of K number of P-bit wide output ports from each of said port blocks of said M number of columns; and

an N x 1 multiplexer for selecting one of N number of output ports selected by said M number of K x 1 multiplexers.

10. The switch of Claim 6 wherein said plurality of port blocks are organized as an array of N number of rows and M number of columns, each of said port blocks having K number of P-bit wide input ports, and said write decoder comprises:

for each of N number of rows, a 1 x M demultiplexer for selecting an input port from a selected one of said port blocks of said M number of columns: and

a 1 x N demultiplexer for selecting between inputs from each of said 1 x M demultiplexers.

11. The switch of Claim 6 wherein said memory cells comprise dynamic random access memory cells.

12. The switch of Claim 6 wherein each of said plurality of memory cells of each said port block is coupled to a plurality of output I/O ports and an input I/O port.

13. The switch of Claim 6 wherein each of said plurality of memory cells of each said port block is coupled to a plurality of input I/O ports and an output port.

14. A switch comprising

a plurality of port blocks organized in an array of N rows and M columns, each said port block comprising

a first P-line wide port;

a plurality of K number of P-line wide second ports; and

a plurality of P number of memory cells each having a first pass gate for selectively coupling said cell to a corresponding one of said lines of said P-line wide first port and a plurality of K number of second pass gates each for selectively coupling said cell to a corresponding line of said P-line wide second ports;

first decoder circuitry comprising:

for each of said N number of rows, M number of K x 1 multiplexers each for selecting one of said K number of P-bit wide second ports from each of said port blocks of said M number of columns; and

an N x 1 multiplexer for selecting one of N number of ports selected by said M number of K x 1 multiplexers; and

second decoder circuitry comprising:

for each of said N number of rows, a 1 x M demultiplexer for selecting one of said first ports of said port blocks of said M number of columns: and

a 1 x N demultiplexer for selecting one of N number of first ports selected by said 1 x M demultiplexer.

15. The switch of Claim 14 wherein said first port of said port blocks comprises an input port and said second decoder comprises a read decoder.

16 The switch of Claim 14 wherein said plurality of second ports of said port locks comprise output ports and said first decoder comprises a write decoder.

17. The switch of Claim 14 wherein said first port of a selected one of said port blocks comprises an output port and said plurality of second ports of said selected one of said port blocks comprise output ports.

18. The switch of Claim 14 wherein said first and second pass gates of a selected one of said memory cells of a selected one of said port blocks selectively couple said first and second ports to a storage capacitor.

19. The switch of Claim 14 wherein:

a first one of said plurality of pass gates of a first selected one of said memory cells of a selected port block couples said first selected memory cell to a first line of a first one of said second ports and a second one of said plurality of pass gates couples said first selected memory cell with a first line of a second one of said second ports; and

a first one of said plurality of pass gates of a second selected one of said memory cells of said selected port block couples said second selected memory cell with a second line of said first one of said second ports and a second one of said pass gates of said second selected memory couples said second selected memory cells with a second line of said second one of said second ports.

20. The switch of Claim 14 wherein said pass gates of said memory cells comprise transistors.